

Patent Abstracts of Japan

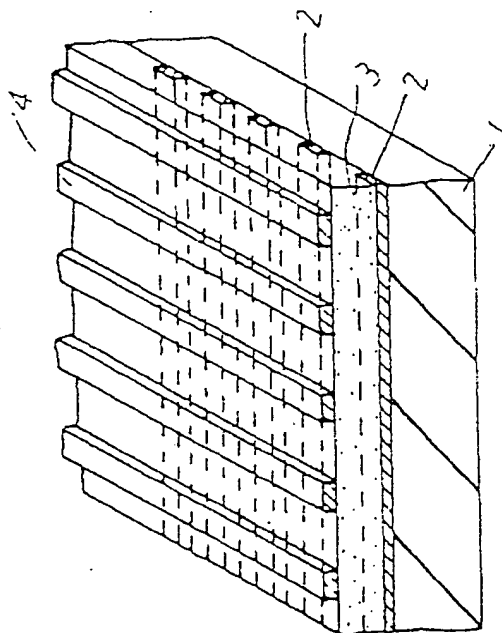
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 PATENTEE : HITACHI SEISAKUSHO KK
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TITLE : MEMORY DEVICE



ABSTRACT : PURPOSE: To enable the increase in integration by a method wherein, in impressing voltage across arbitrary electrodes rectangularly intersecting by sandwiching an amorphous Si layer on an insulation substrate, a memory circuit is constructed by utilizing the variation in the resistance of the amorphous Si layer between the electrodes.
 CONSTITUTION: In the device having electrode arrays rectangularly intersecting to each other by sandwiching the amorphous Si layer 3, a voltage is impressed across an arbitrary electrode of the first electrode array and an arbitrary electrode of the second electrode array; when the voltage becomes over a specific one, the amorphous Si at the part of electrode intersection varies, and then the resistance of the region reduces locally and rapidly. It becomes possible to use this device as a writable nonvolatile memory by utilizing such an electric characteristic of the amorphous Si. Besides, the layer multiplication of memory layer becomes facilitated, which becomes much more advantageous for the increase in integration.